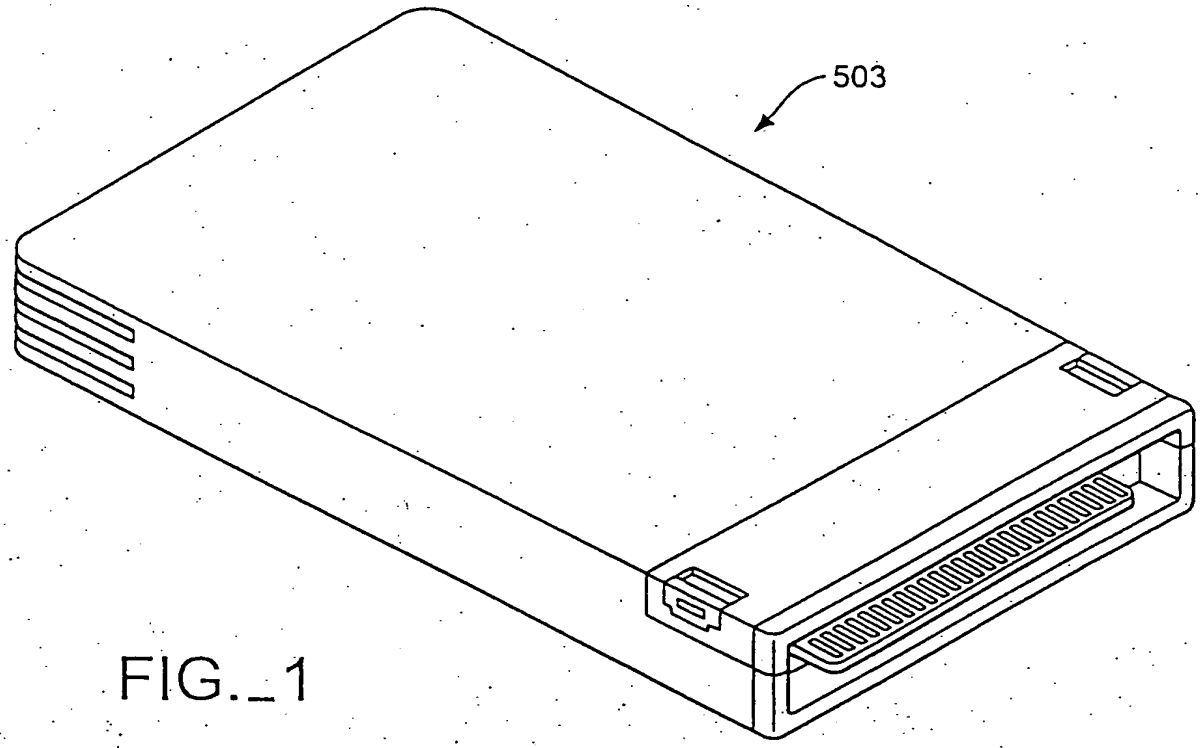


FIG._1

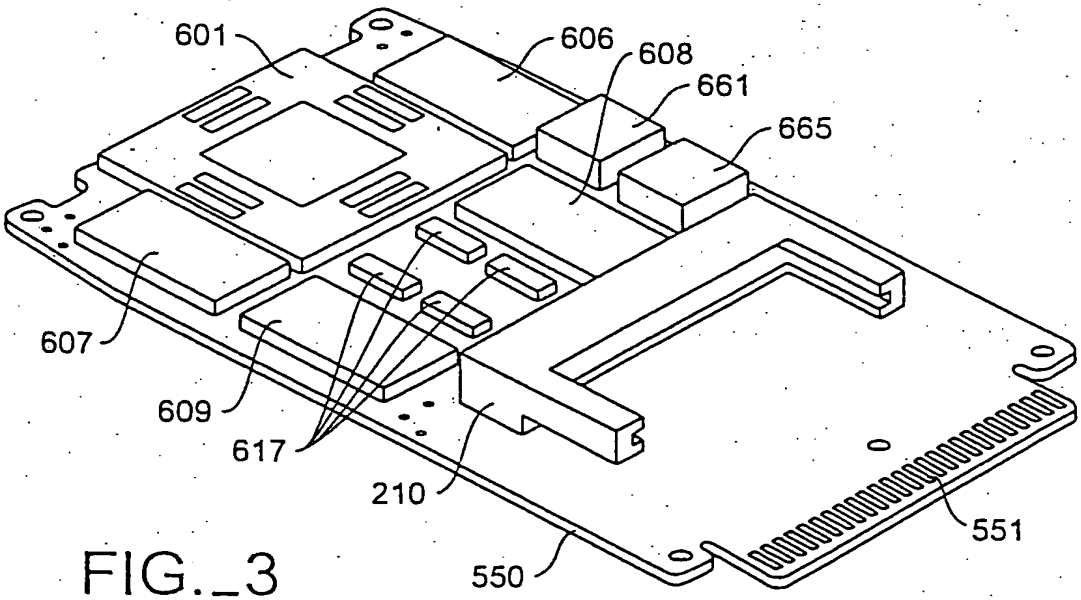
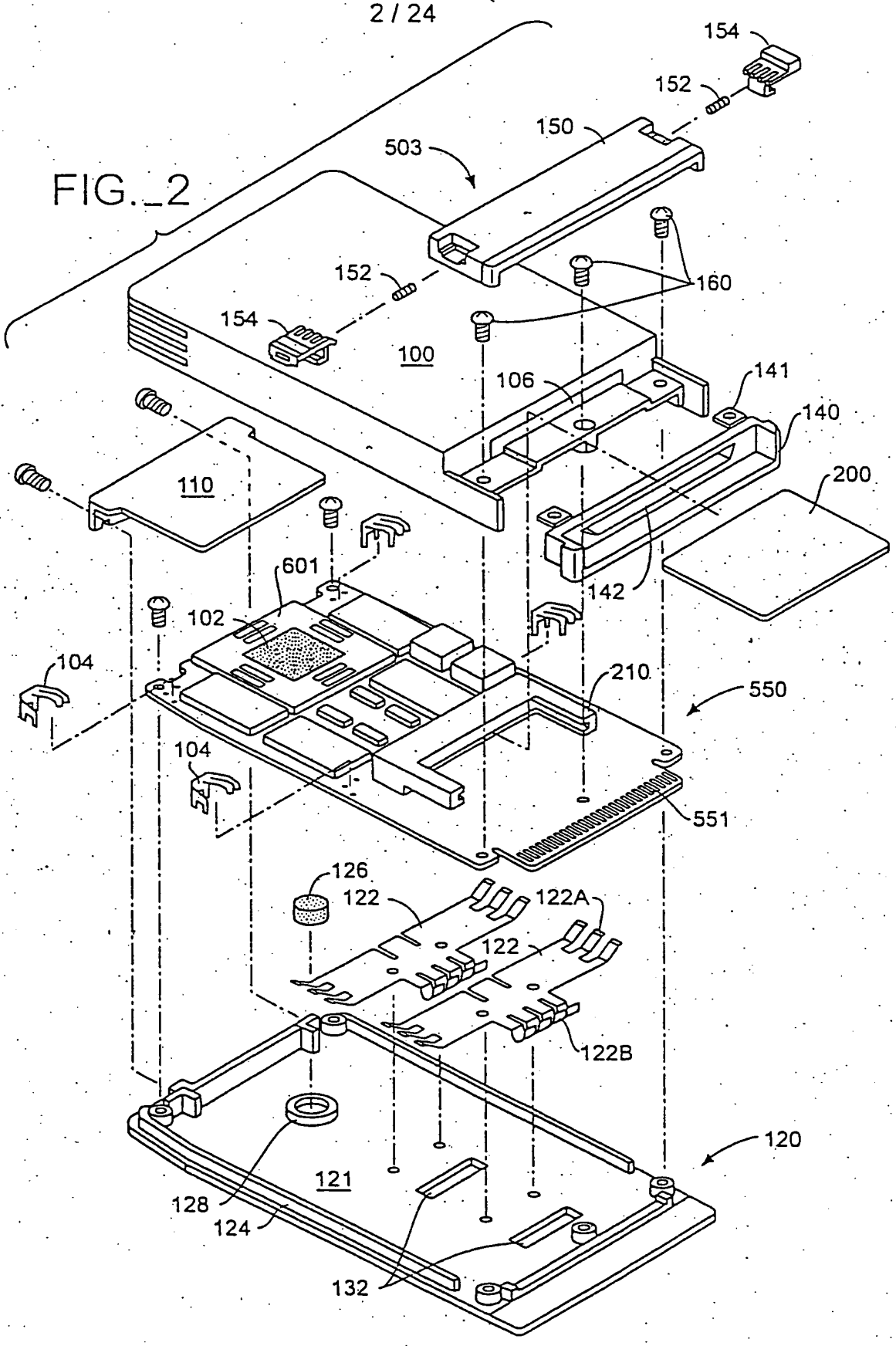


FIG._3

FIG._2


154
152
150
503
160
152
154
100
106
141
140
110
200
601
142
102
104
210
550
104
551
126
122
122A
122
122B
120
121
128
124
132

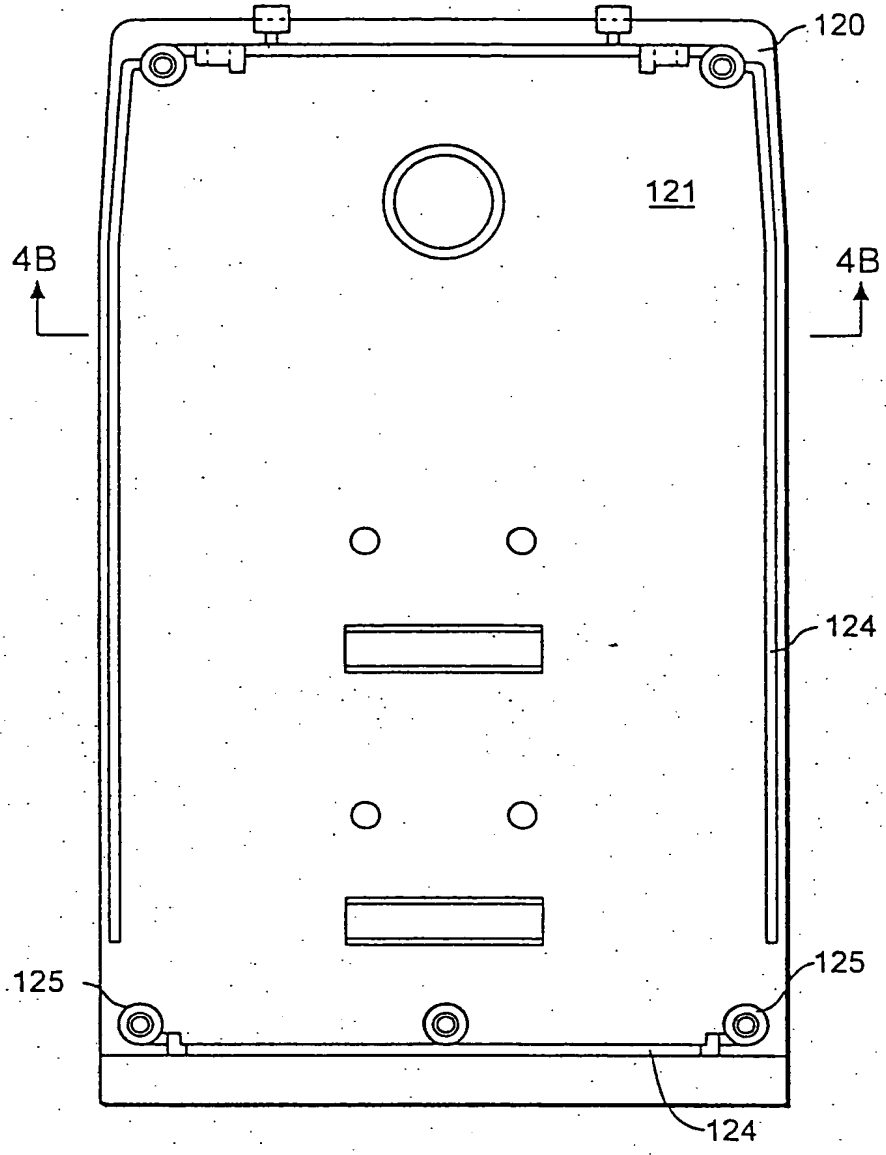


FIG._4A

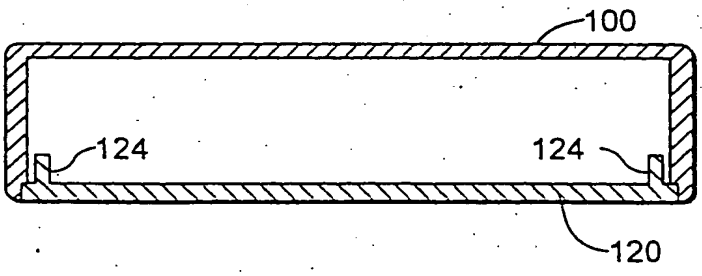


FIG._4B

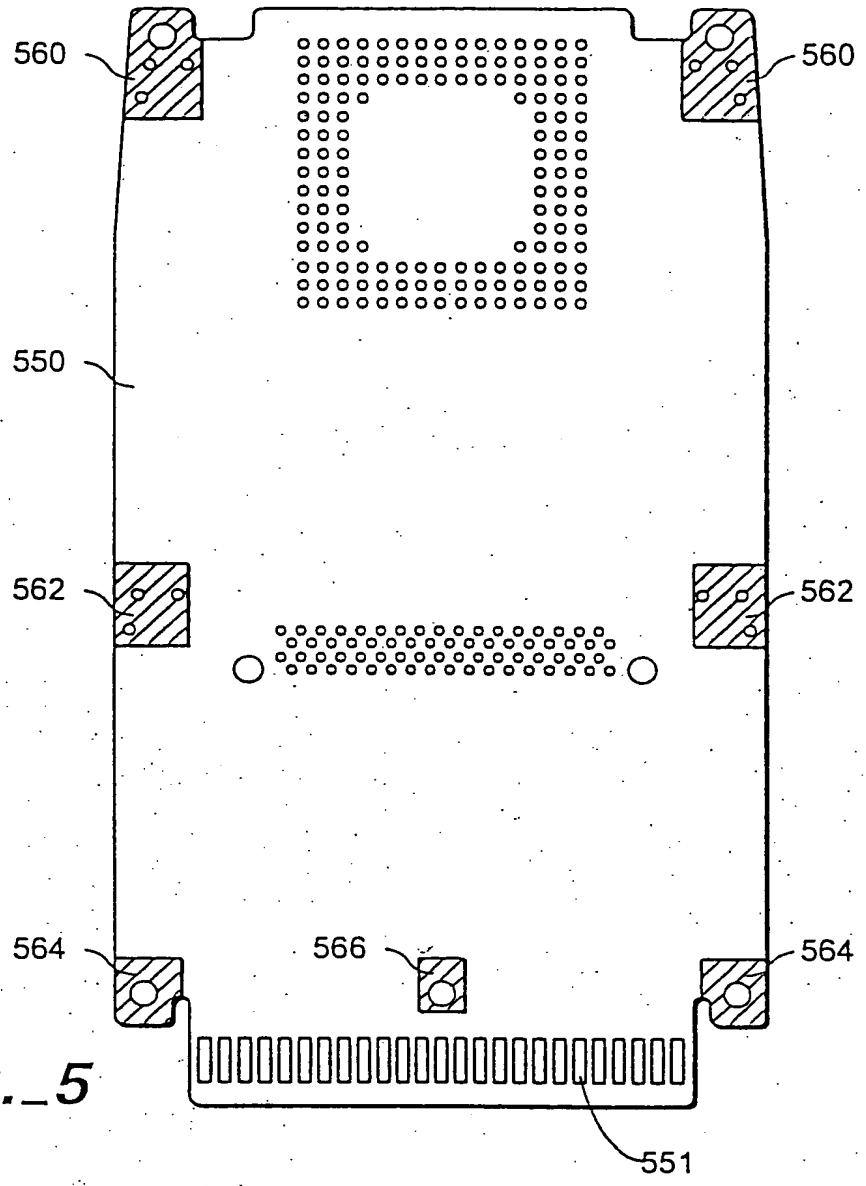

560
560
550
562
562
564
566
564
551

FIG._5

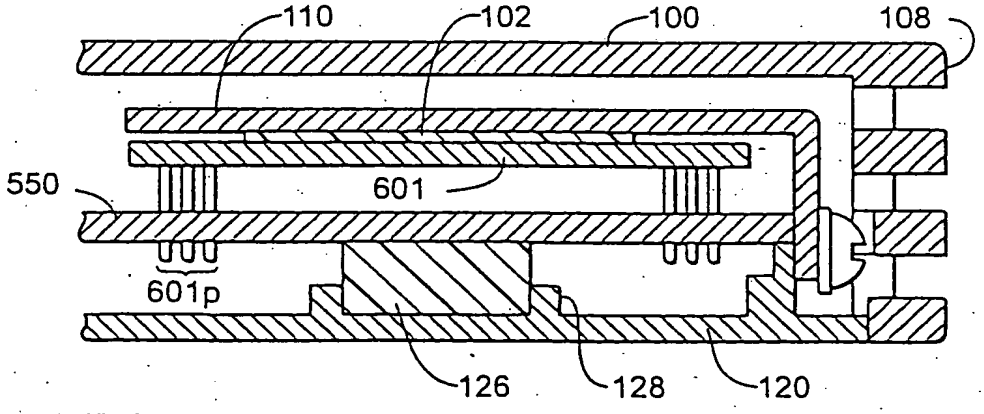

110
102
100
108
550
601
601p
126
128
120

FIG._7

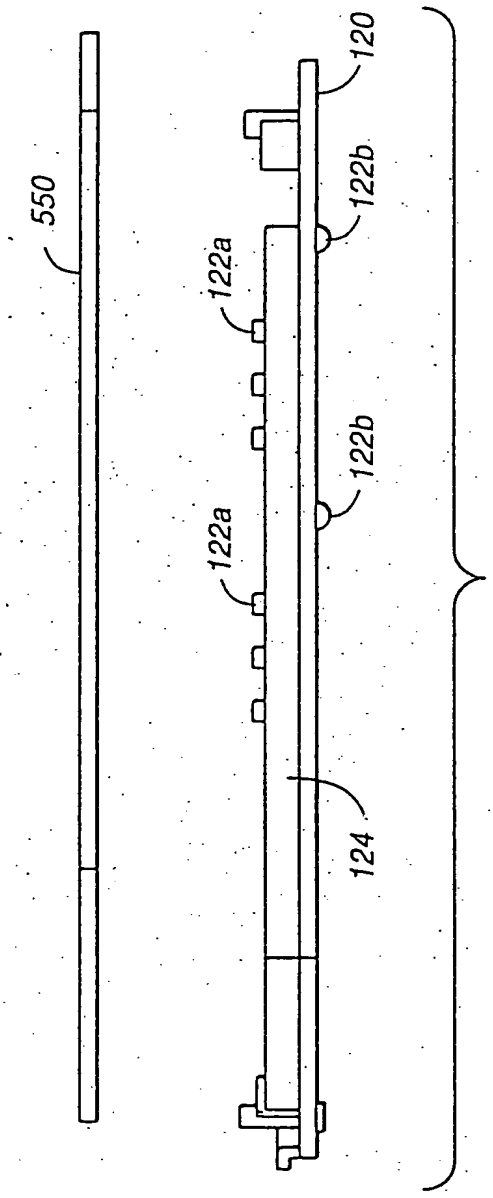


FIG._6A

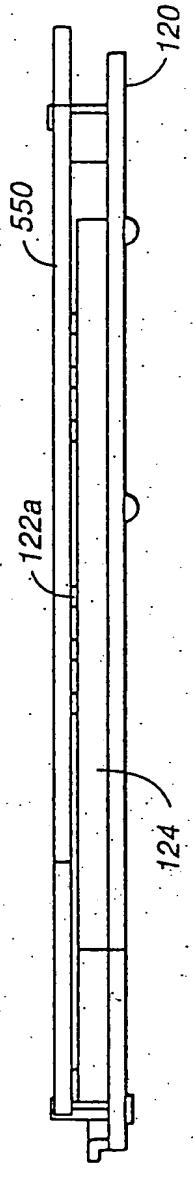


FIG._6B

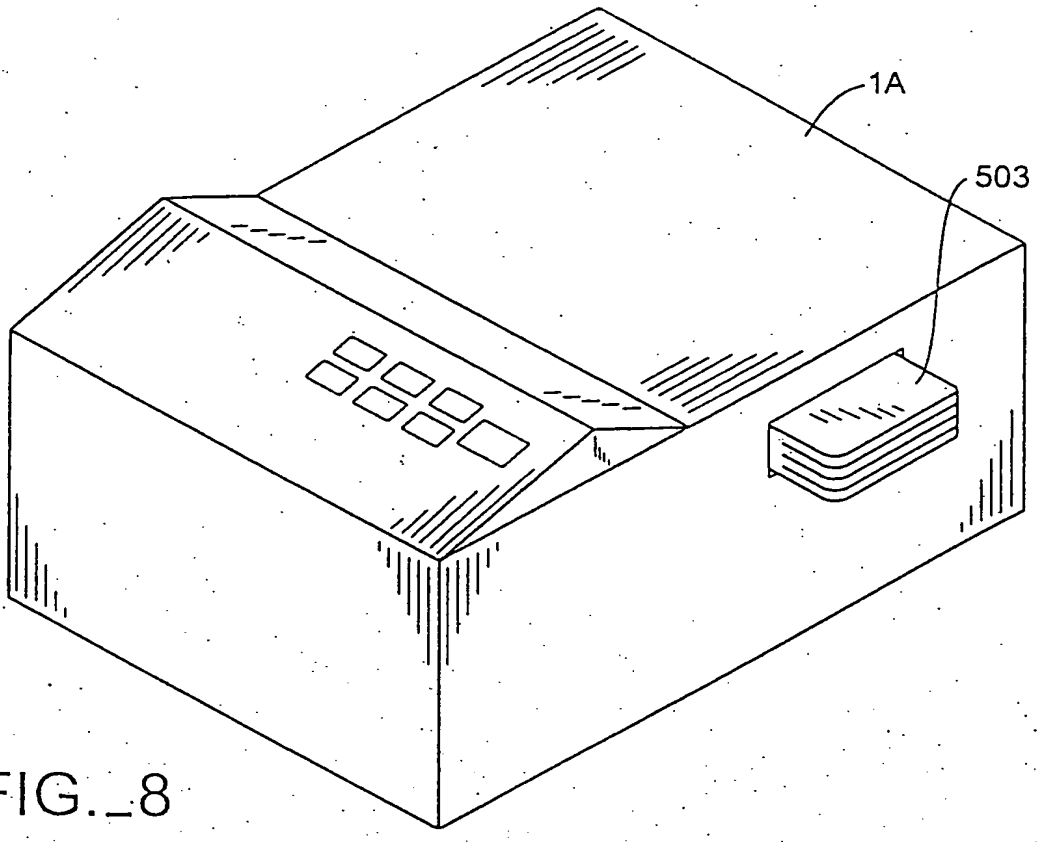


FIG._8

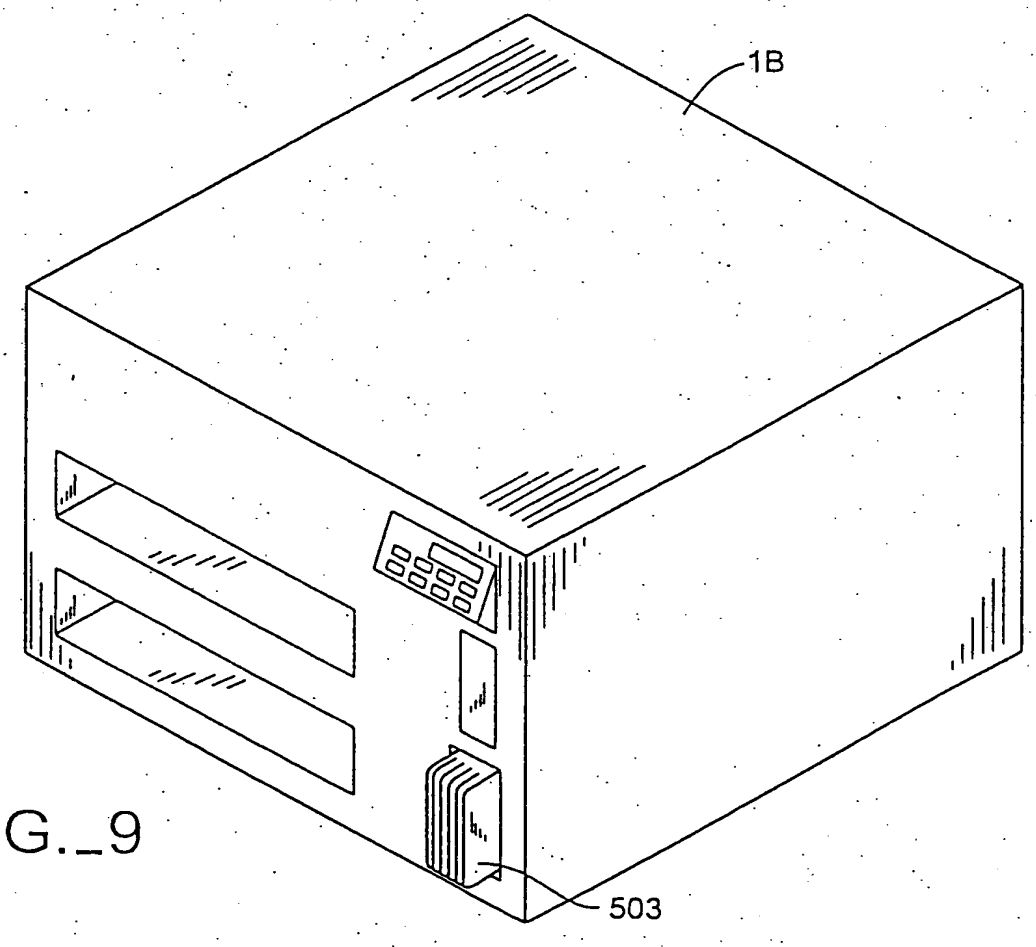


FIG._9

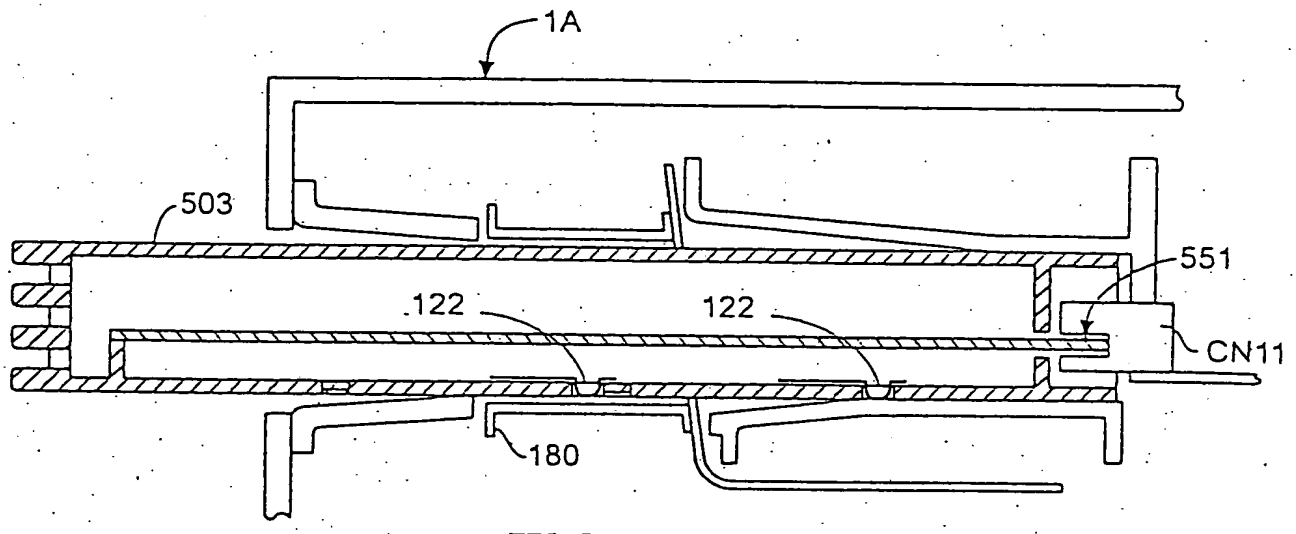


FIG._10

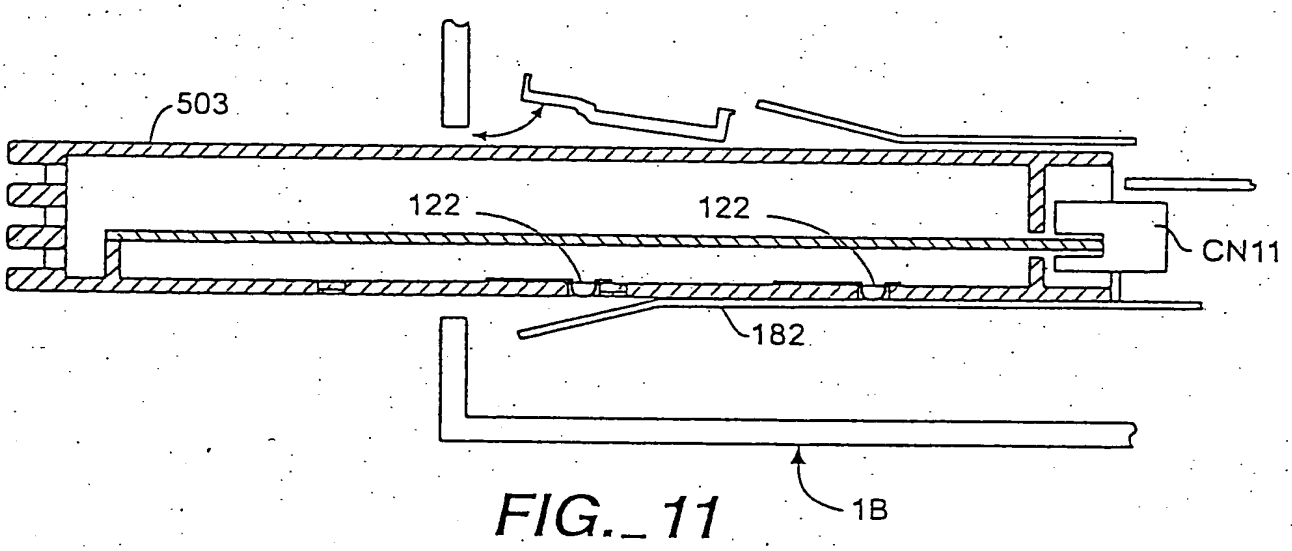


FIG._11

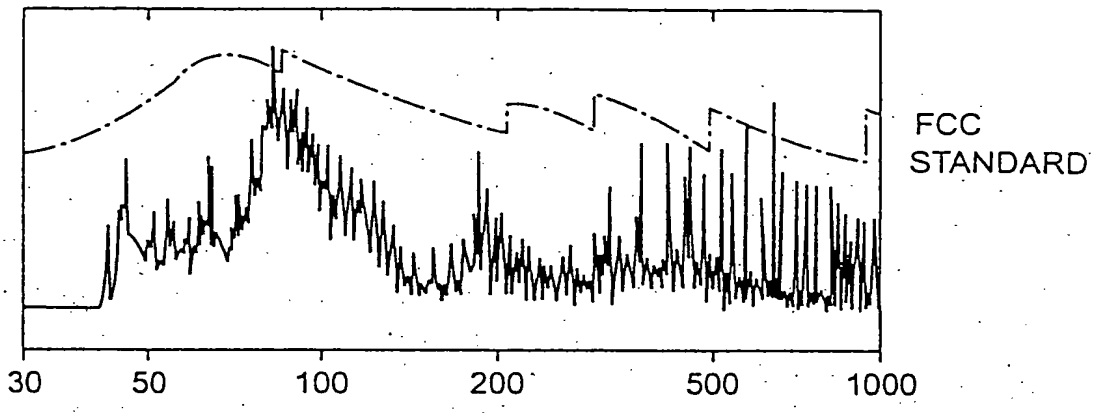


FIG._12A

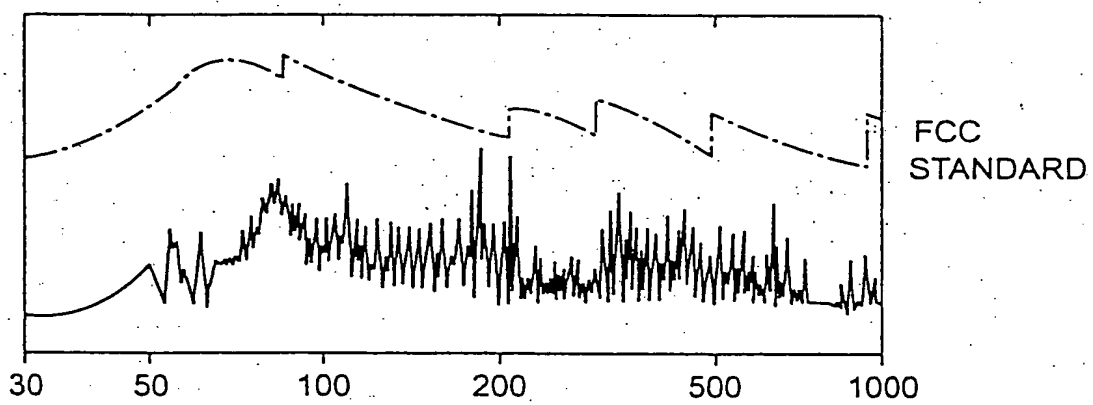


FIG._12B

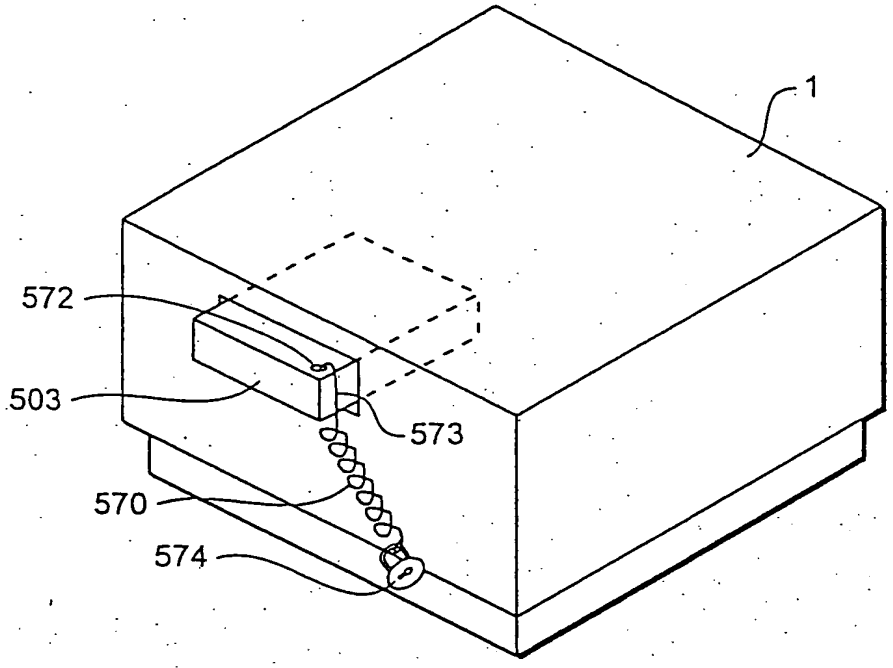


FIG._13

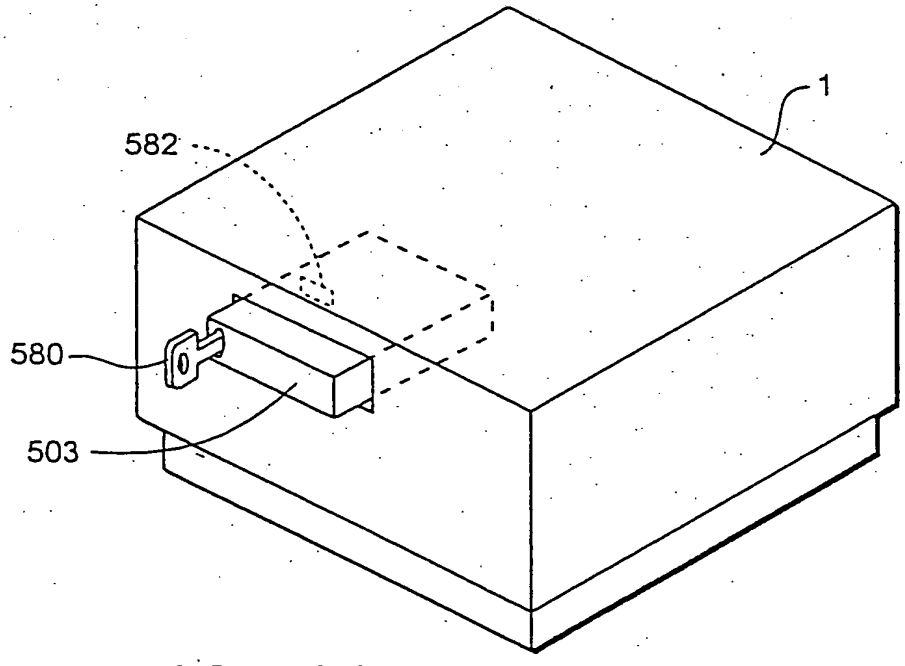


FIG._14

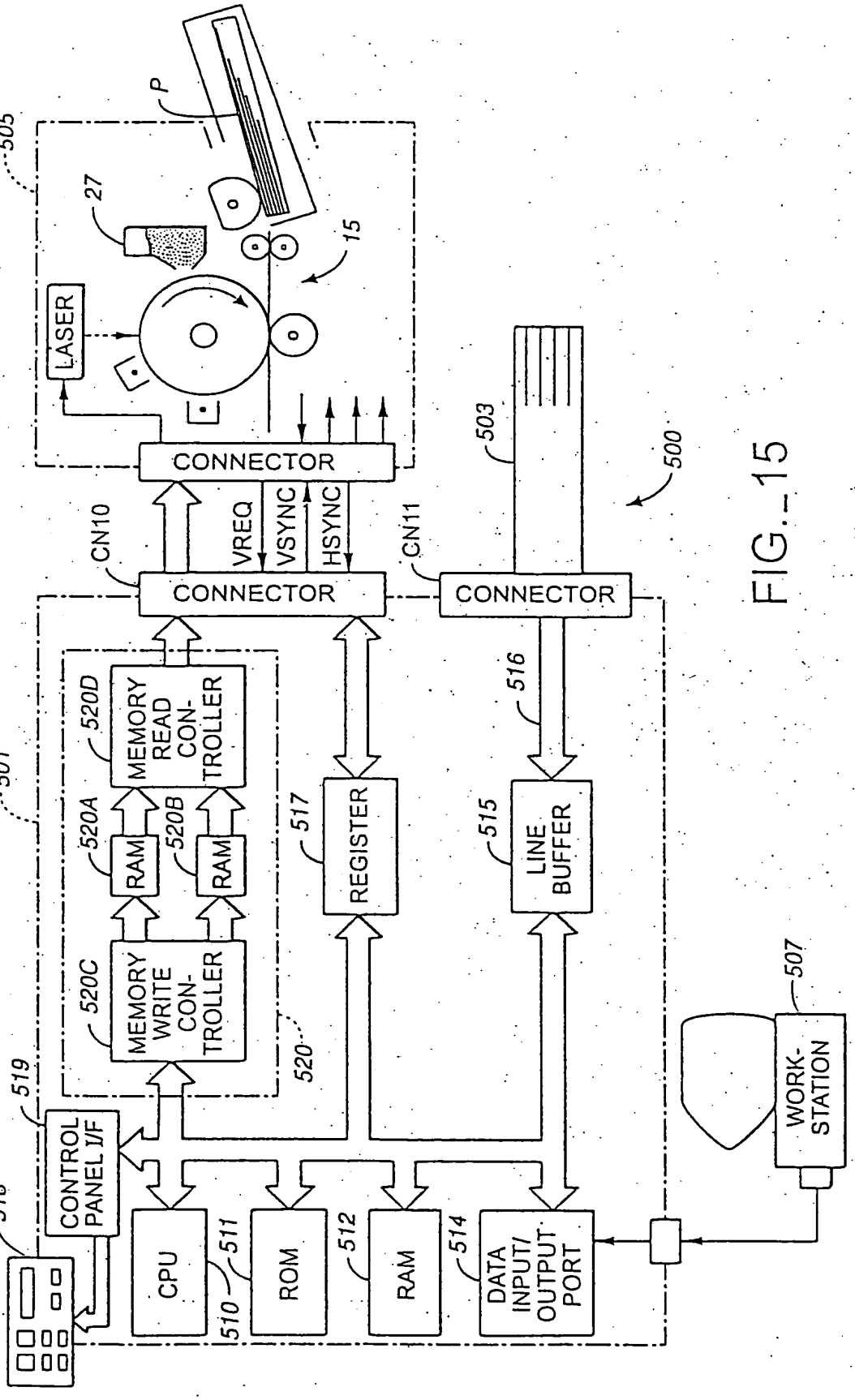

P
505
27
15
LASER
CONNECTOR
VREQ
VSYNC
HSYNC
CN10
CN11
CONNECTOR
CONNECTOR
503
500
501
520D
MEMORY READ CON-TROLLER
520A
RAM
520B
RAM
520C
MEMORY WRITE CON-TROLLER
520
517
REGISTER
516
515
LINE BUFFER
507
WORK-STATION
519
CONTROL PANEL I/F
518
CPU
511
510
ROM
512
RAM
514
DATA INPUT/ OUTPUT PORT

FIG._15

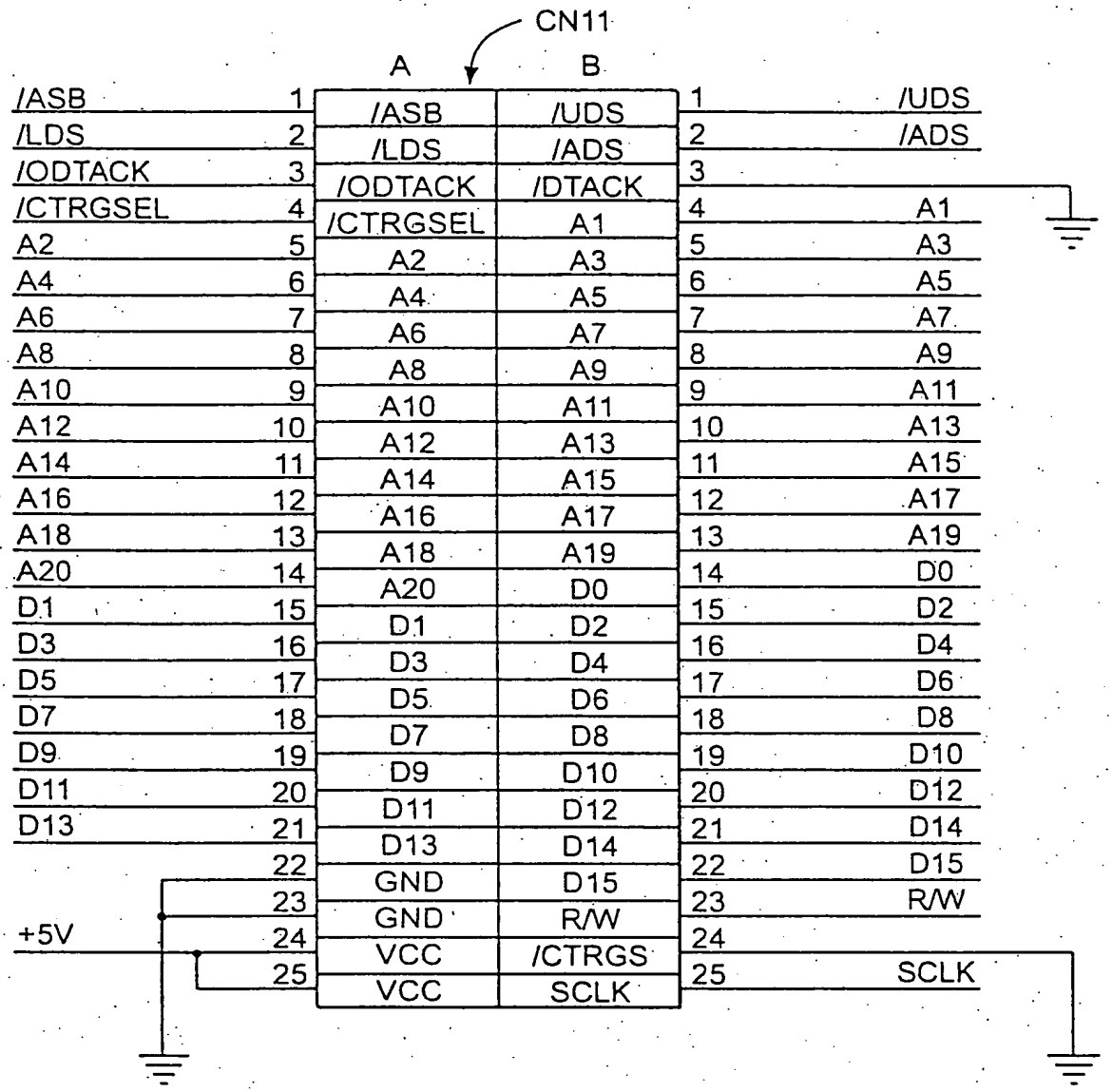

CN11
A
B
/ASB 1 /ASB /UDS 1 /UDS
/LDS 2 /LDS /ADS 2 /ADS
/ODTACK 3 /ODTACK /DTACK 3
/CTRGSEL 4 /CTRGSEL A1 4 A1
A2 5 A2 A3 5 A3
A4 6 A4 A5 6 A5
A6 7 A6 A7 7 A7
A8 8 A8 A9 8 A9
A10 9 A10 A11 9 A11
A12 10 A12 A13 10 A13
A14 11 A14 A15 11 A15
A16 12 A16 A17 12 A17
A18 13 A18 A19 13 A19
A20 14 A20 D0 14 D0
D1 15 D1 D2 15 D2
D3 16 D3 D4 16 D4
D5 17 D5 D6 17 D6
D7 18 D7 D8 18 D8
D9 19 D9 D10 19 D10
D11 20 D11 D12 20 D12
D13 21 D13 D14 21 D14
22 GND D15 22 D15
23 GND R/W 23 R/W
+5V 24 VCC /CTRGS 24
25 VCC SCLK 25 SCLK

FIG._16

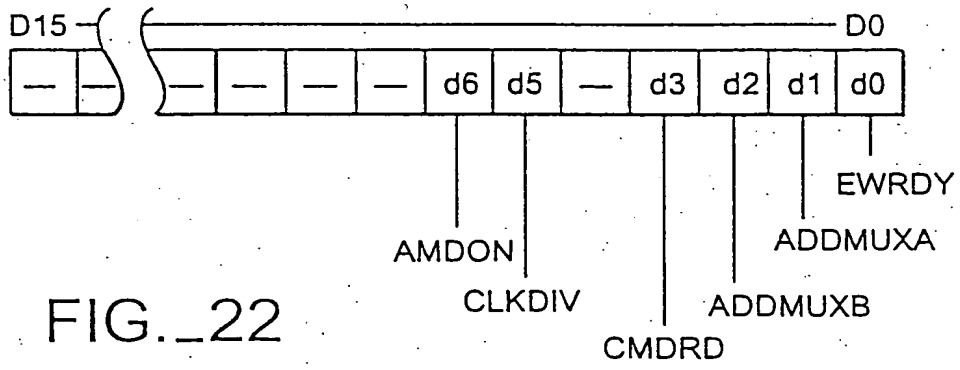

D15
D0
d6
d5
d3
d2
d1
d0
EWRDY
AMDON
CLKDIV
CMDRD
ADDMUXB
ADDMUXA

FIG._22

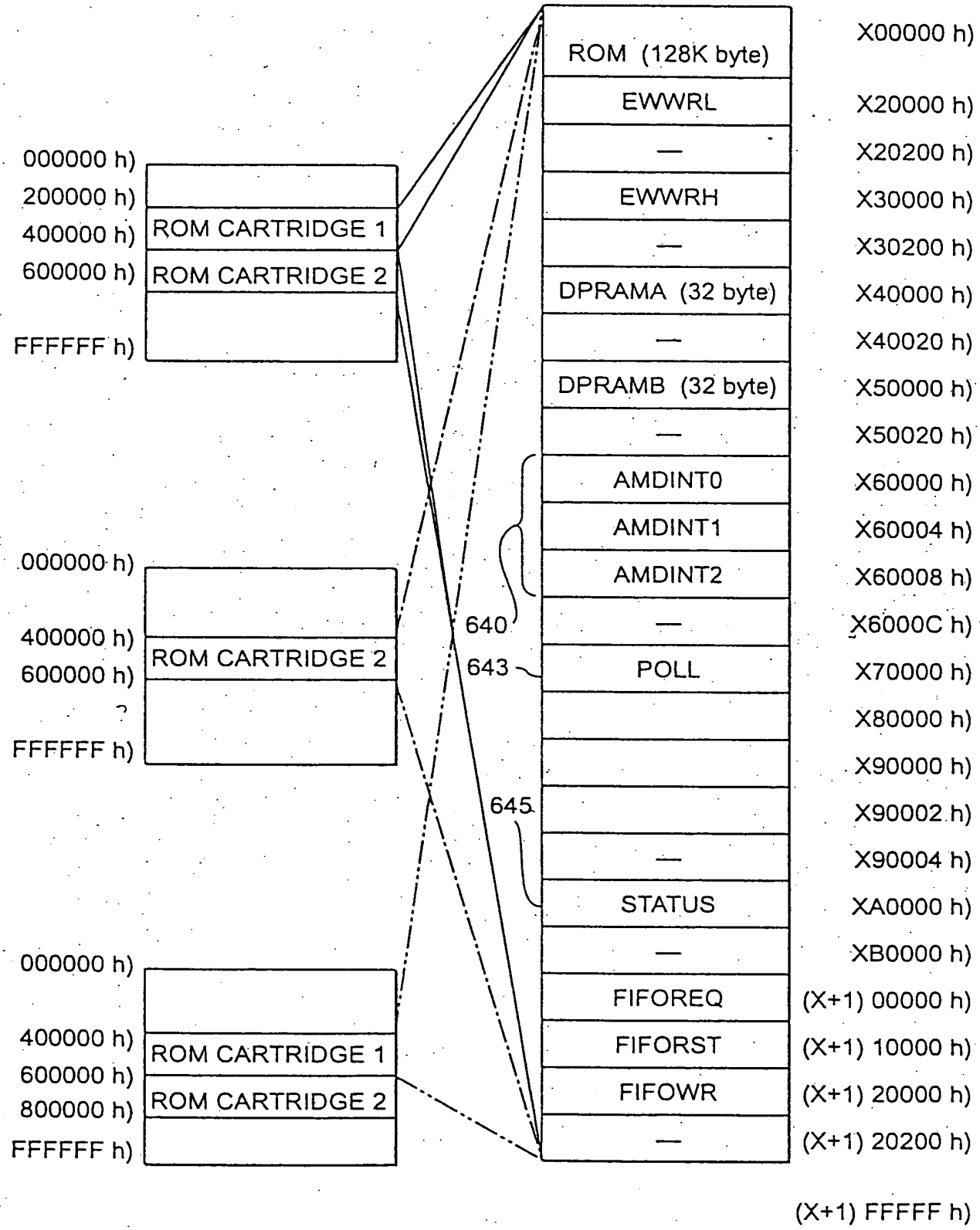

000000 h)
200000 h)
400000 h)
600000 h)
FFFFFF h)
ROM CARTRIDGE 1
ROM CARTRIDGE 2
000000 h)
400000 h)
600000 h)
FFFFFF h)
ROM CARTRIDGE 2
000000 h)
400000 h)
600000 h)
800000 h)
FFFFFF h)
ROM CARTRIDGE 1
ROM CARTRIDGE 2
640
643
645
ROM (128K byte)
EWWRL
—
EWWRH
—
DPRAMA (32 byte)
—
DPRAMB (32 byte)
—
AMDINT0
AMDINT1
AMDINT2
—
POLL
STATUS
—
FIFOREQ
FIFORST
FIFOWR
—
X00000 h)
X20000 h)
X20200 h)
X30000 h)
X30200 h)
X40000 h)
X40020 h)
X50000 h)
X50020 h)
X60000 h)
X60004 h)
X60008 h)
X6000C h)
X70000 h)
X80000 h)
X90000 h)
X90002 h)
X90004 h)
XA0000 h)
XB0000 h)
(X+1) 00000 h)
(X+1) 10000 h)
(X+1) 20000 h)
(X+1) 20200 h)
(X+1) FFFFF h)

FIG._17

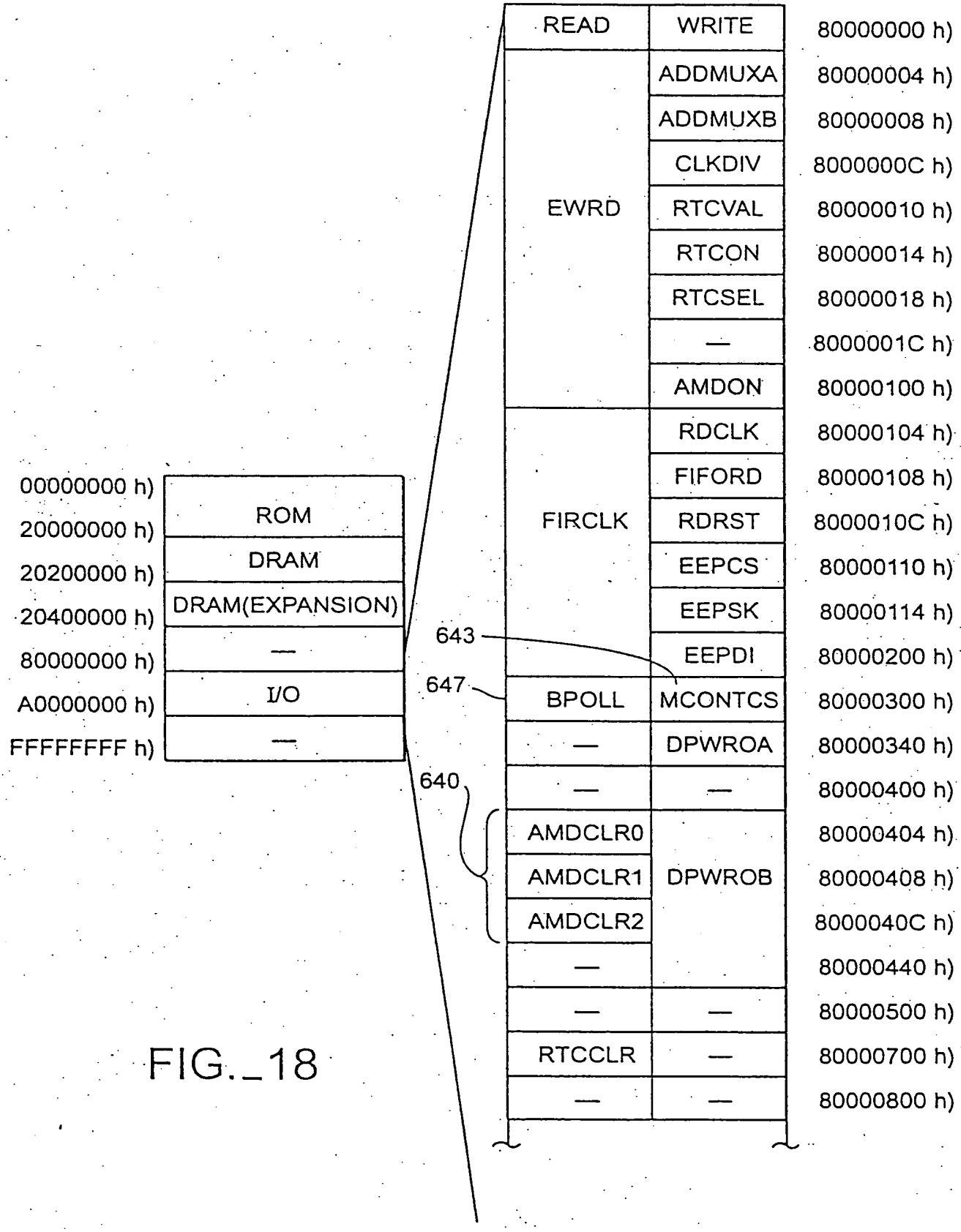

00000000 h)
20000000 h)
20200000 h)
20400000 h)
80000000 h)
A0000000 h)
FFFFFFFF h)
ROM
DRAM
DRAM(EXPANSION)
—
I/O
—
643
647
640
READ
WRITE
80000000 h)
EWRD
ADDMUXA
80000004 h)
ADDMUXB
80000008 h)
CLKDIV
8000000C h)
RTCVAL
80000010 h)
RTCON
80000014 h)
RTCSEL
80000018 h)
—
8000001C h)
AMDON
80000100 h)
FIRCLK
RDCLK
80000104 h)
FIFORD
80000108 h)
RDRST
8000010C h)
EEPCS
80000110 h)
EEPSK
80000114 h)
EEPDI
80000200 h)
BPOLL
MCONTCS
80000300 h)
—
DPWROA
80000340 h)
—
—
80000400 h)
AMDCLR0
DPWROB
80000404 h)
AMDCLR1
80000408 h)
AMDCLR2
8000040C h)
—
80000440 h)
—
—
80000500 h)
RTCCLR
—
80000700 h)
—
—
80000800 h)

FIG._18

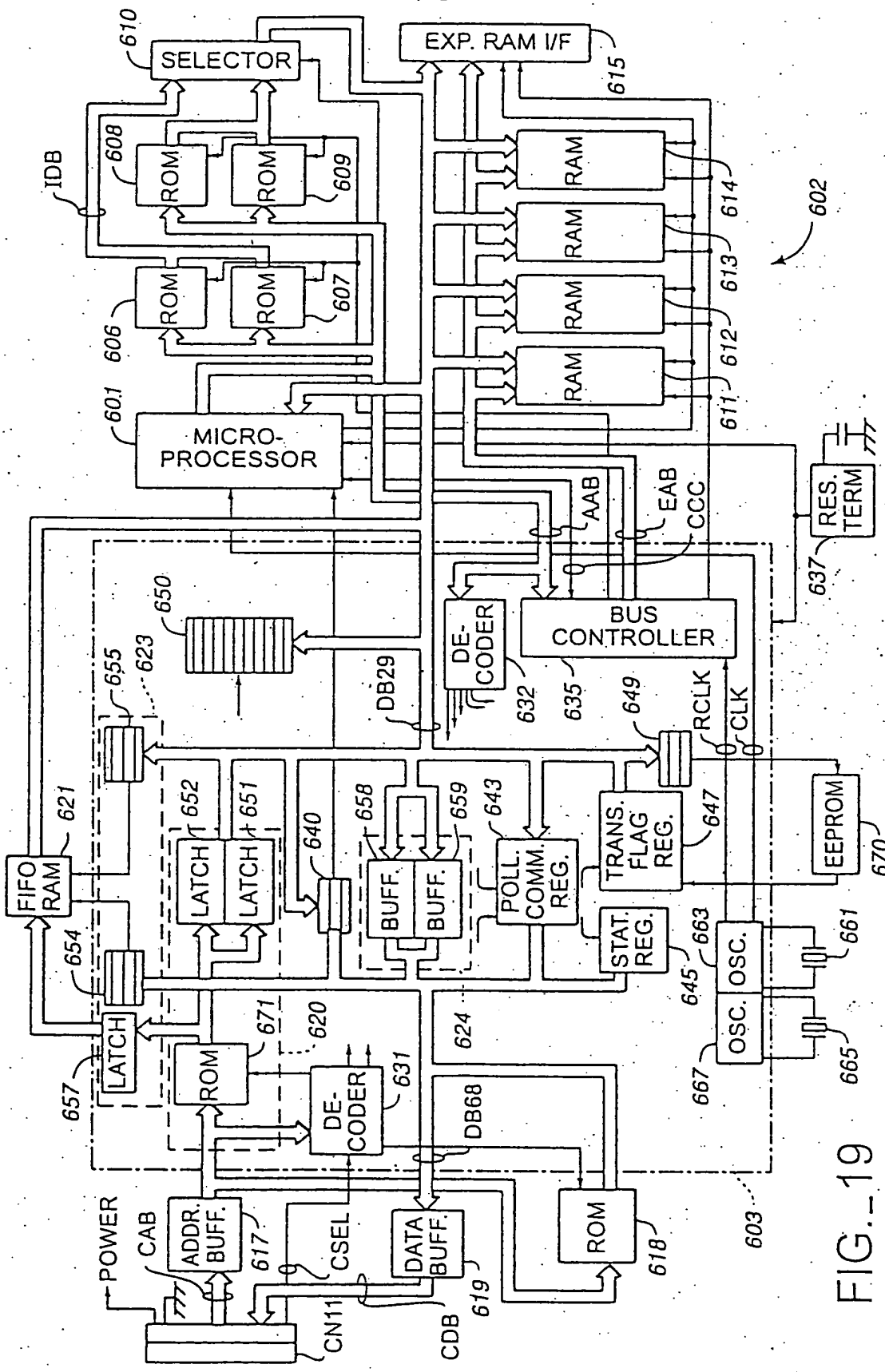

SELECTOR
610
EXP. RAM I/F
615
IDB
608
ROM
609
607
606
601
MICRO-
PROCESSOR
RAM
614
613
612
611
602
AAB
EAB
CCC
RES.
TERM
637
650
623
655
DE-
CODER
632
BUS
CONTROLLER
635
649
DB29
RCLK
CLK
621
652
651
640
658
659
643
647
LATCH
BUFF.
POLL.
COMM.
REG.
TRANS.
FLAG
REG.
EEPROM
670
654
STAT.
REG.
645
663
OSC.
661
665
667
657
671
620
631
624
DB68
603
POWER
CAB
ADDR.
BUFF.
617
CSEL
DATA
BUFF.
619
618
CN11
CDB

FIG._19

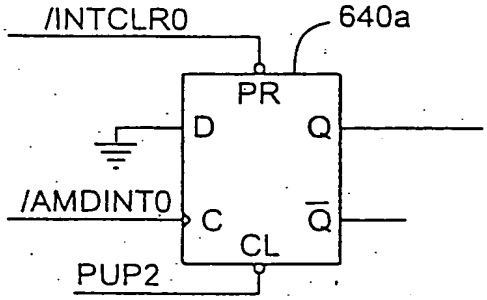


FIG._20A

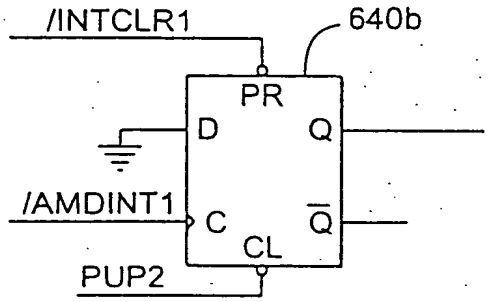


FIG._20B

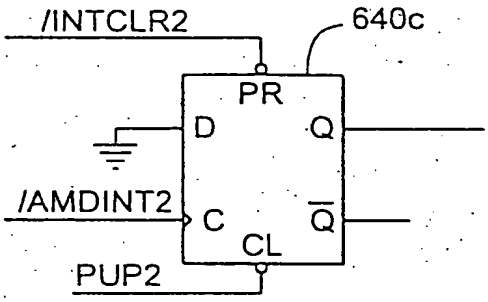


FIG._20C

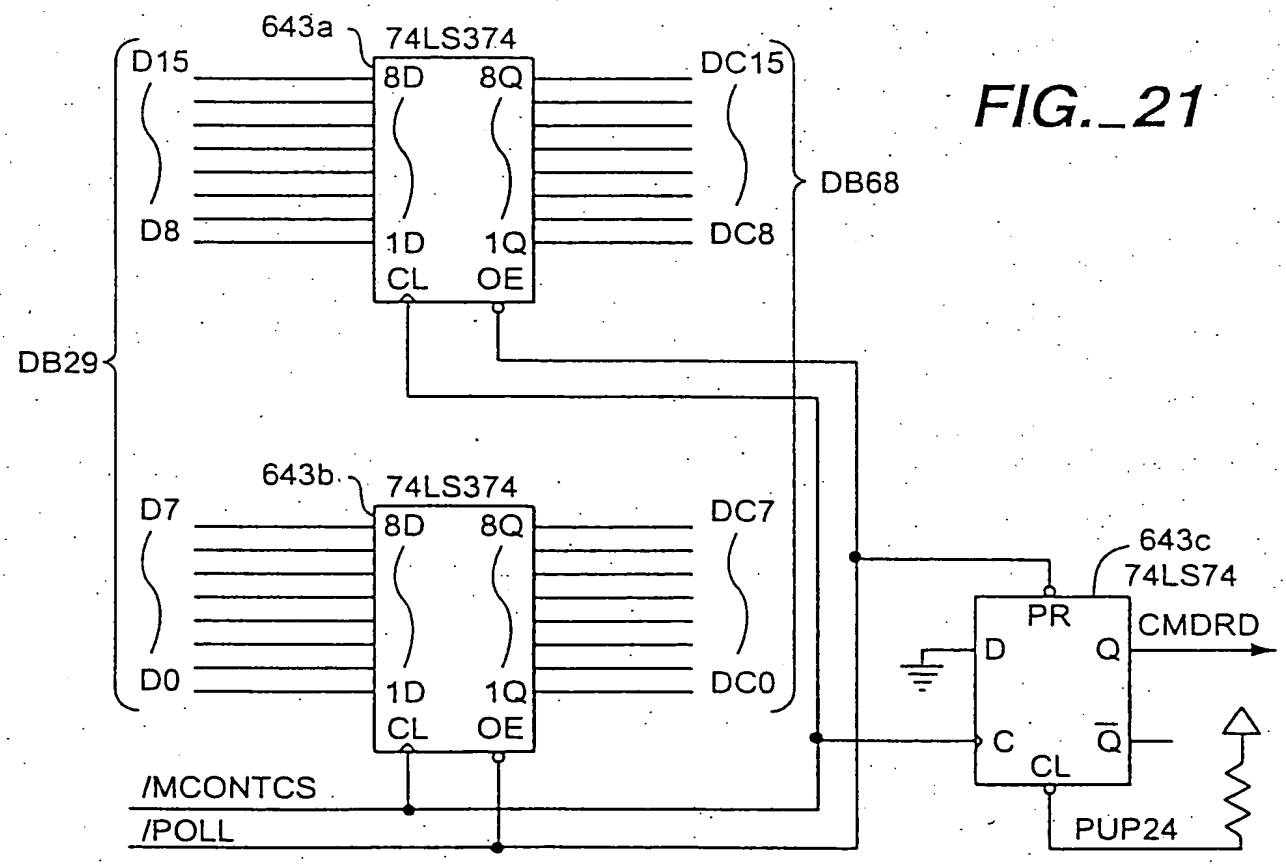
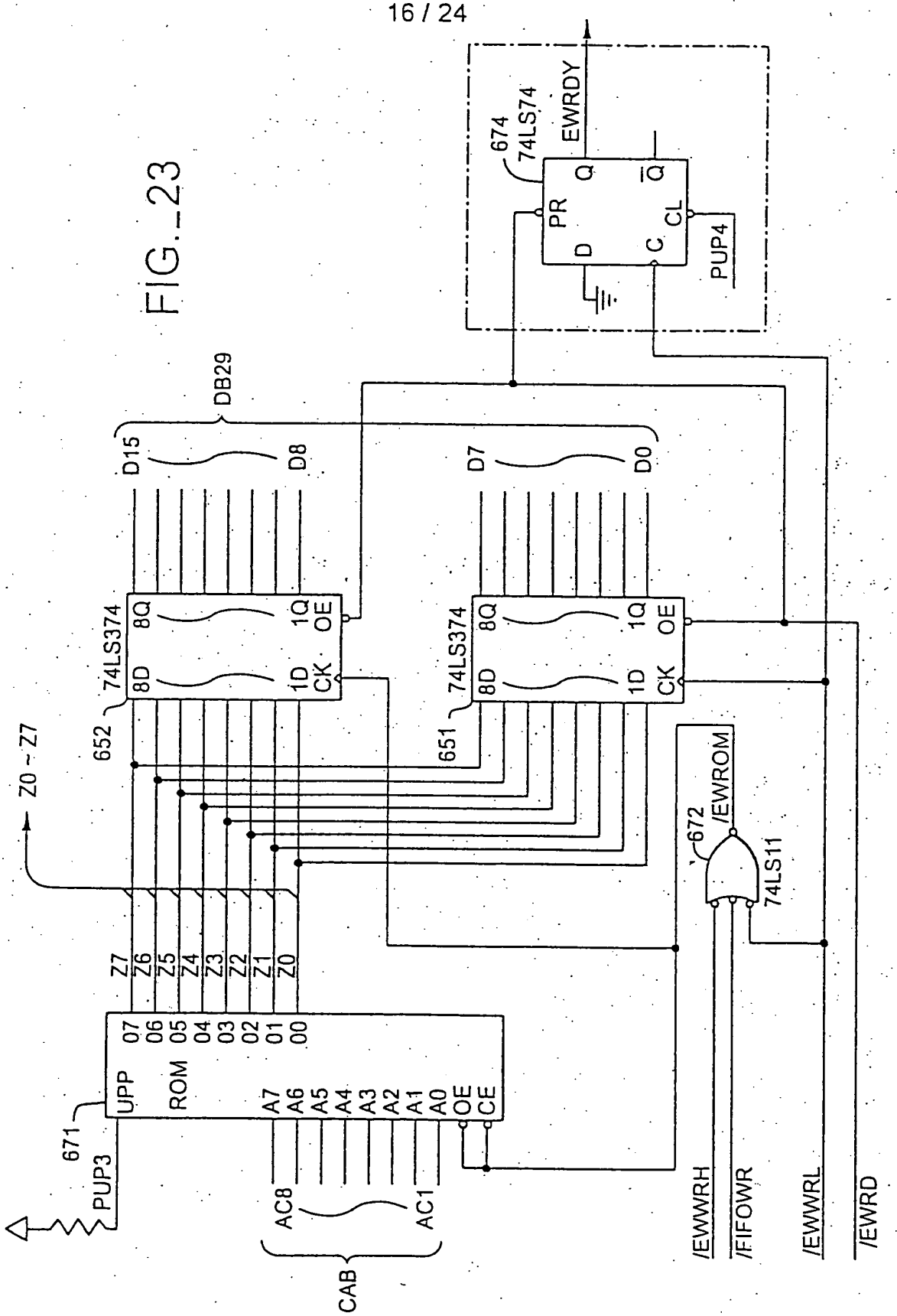


FIG._21

FIG._23


674
74LS74
EWRDY
PR
D
C
CL
PUP4
DB29
D15
D8
D7
D0
74LS374
8D
8Q
1D
1Q
CK
OE
652
651
Z0 ~ Z7
672
/EWROM
74LS11
Z7
Z6
Z5
Z4
Z3
Z2
Z1
Z0
07
06
05
04
03
02
01
00
UPP
ROM
671
PUP3
A7
A6
A5
A4
A3
A2
A1
A0
OE
CE
AC8
AC1
CAB
/EWWRH
/FIFOWR
/EWWRL
/EWRD

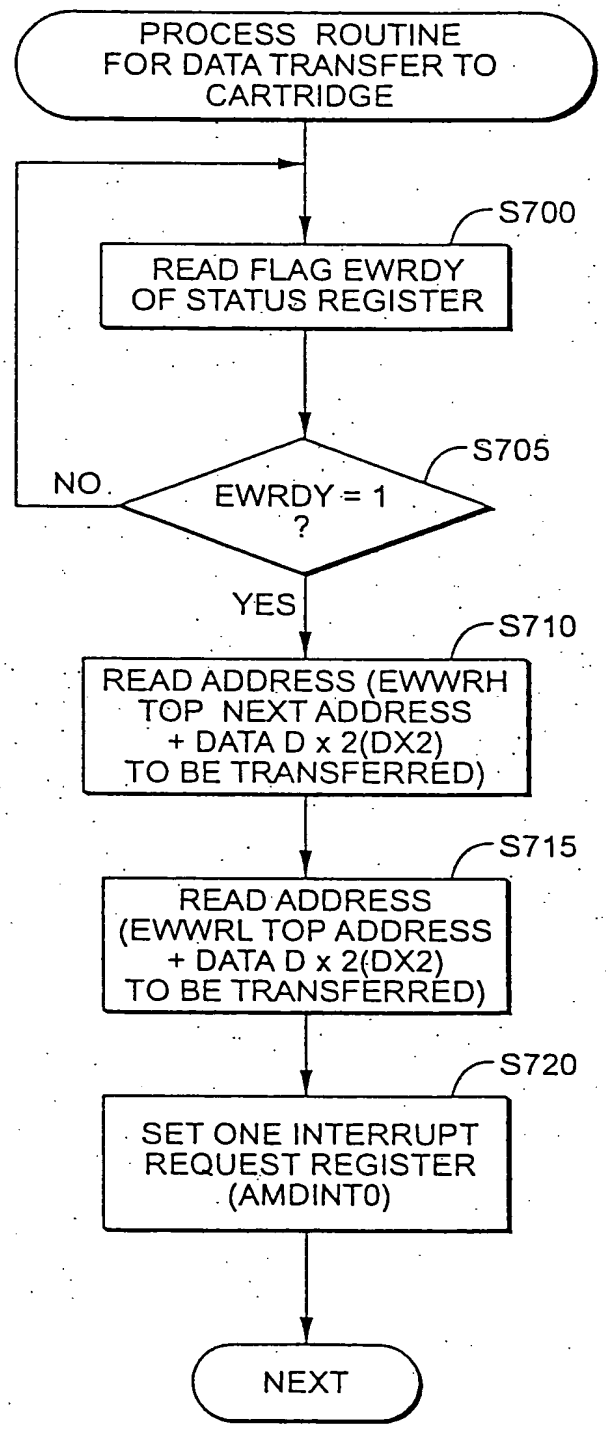


FIG._24

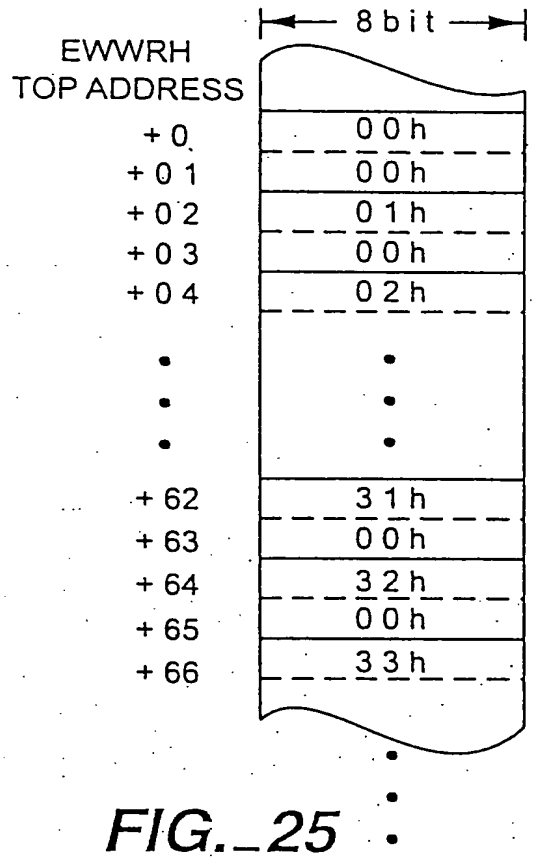


FIG._25

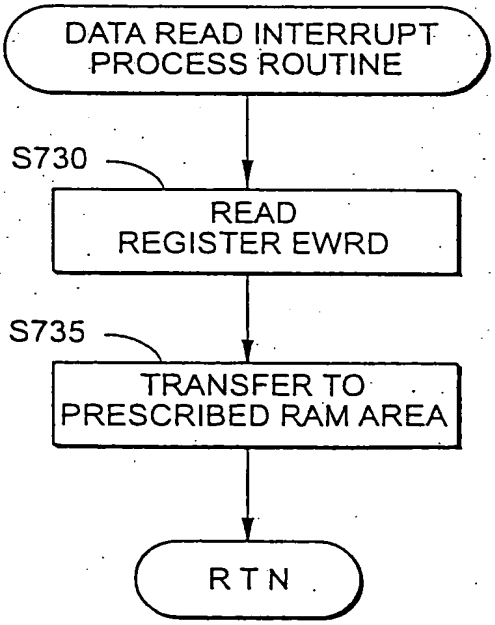


FIG._26

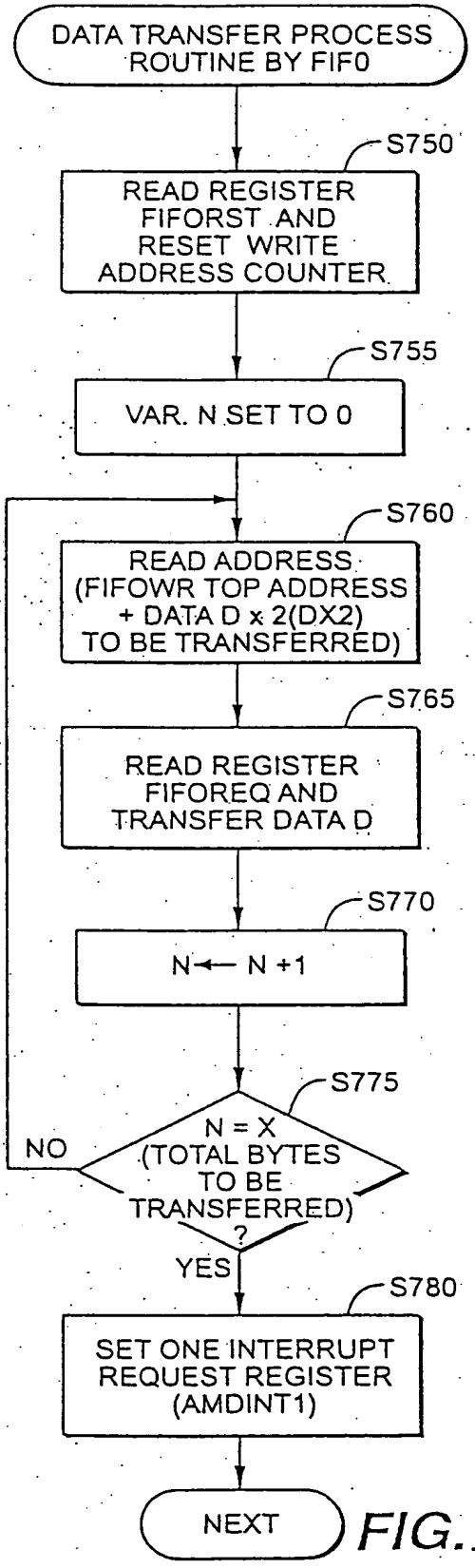

DATA TRANSFER PROCESS ROUTINE BY FIF0
S750
READ REGISTER FIFORST AND RESET WRITE ADDRESS COUNTER
S755
VAR. N SET TO 0
S760
READ ADDRESS (FIFOWR TOP ADDRESS + DATA D x 2(DX2) TO BE TRANSFERRED)
S765
READ REGISTER FIFOREQ AND TRANSFER DATA D
S770
N ← N +1
S775
N = X (TOTAL BYTES TO BE TRANSFERRED) ?
NO
YES
S780
SET ONE INTERRUPT REQUEST REGISTER (AMDINT1)
NEXT

FIG._27

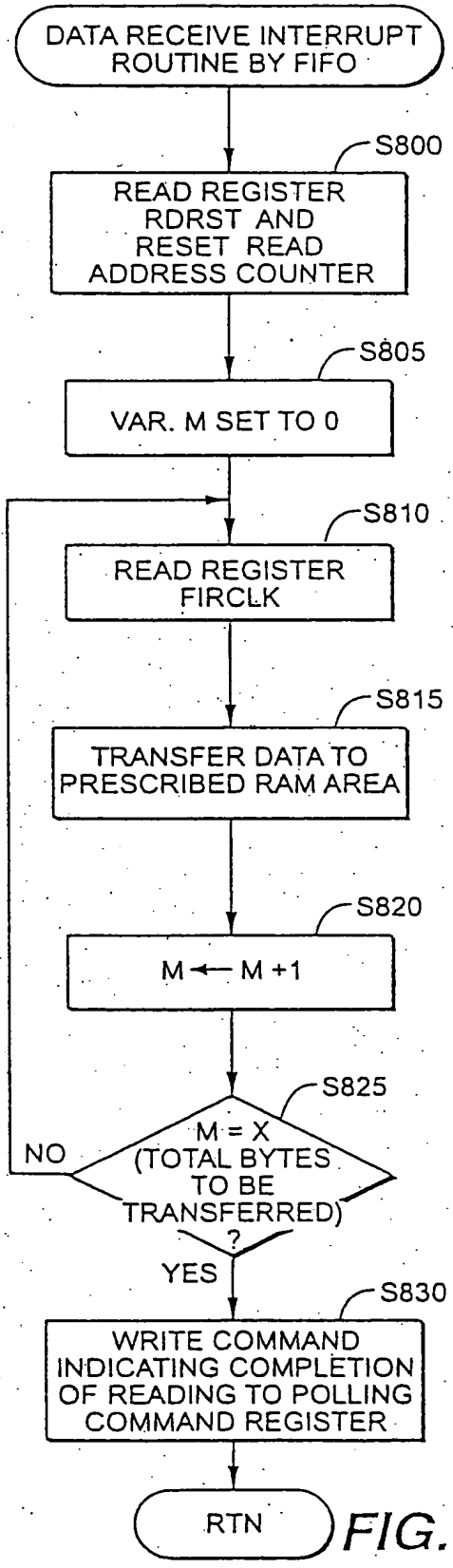

DATA RECEIVE INTERRUPT ROUTINE BY FIFO
S800
READ REGISTER RDRST AND RESET READ ADDRESS COUNTER
S805
VAR. M SET TO 0
S810
READ REGISTER FIRCLK
S815
TRANSFER DATA TO PRESCRIBED RAM AREA
S820
M ← M +1
S825
M = X (TOTAL BYTES TO BE TRANSFERRED) ?
NO
YES
S830
WRITE COMMAND INDICATING COMPLETION OF READING TO POLLING COMMAND REGISTER
RTN

FIG._28

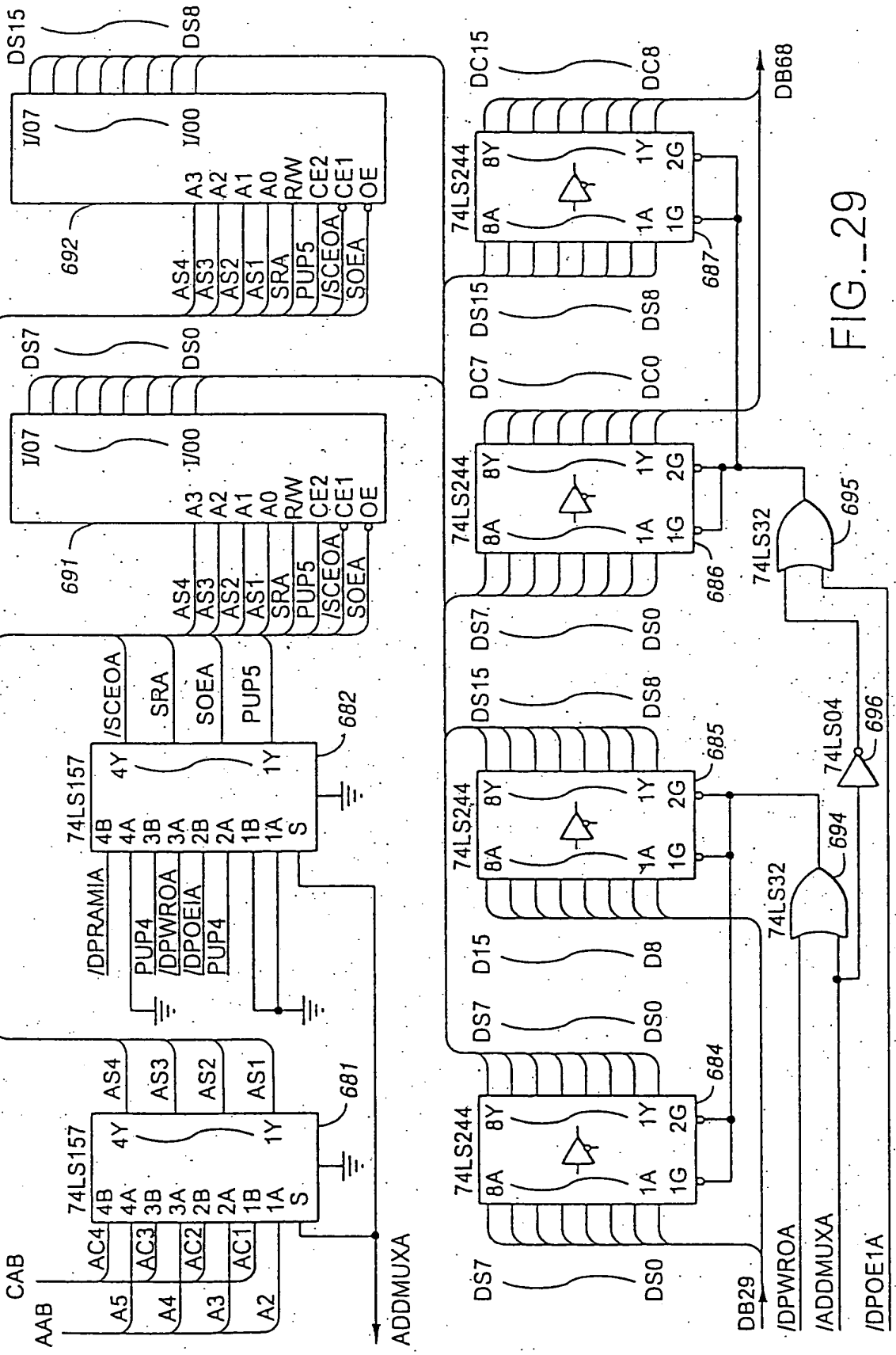

DS15
DS8
I/07
I/00
A3
A2
A1
A0
R/W
CE2
CE1
OE
692
AS4
AS3
AS2
AS1
SRA
PUP5
/SCEOA
SOEA
DS7
DS0
691
74LS157
4B
4A
3B
3A
2B
2A
1B
1A
S
4Y
1Y
682
/SCEOA
SRA
SOEA
PUP5
/DPRAMIA
PUP4
/DPWROA
/DPOEIA
PUP4
681
AC4
AC3
AC2
AC1
CAB
AAB
A5
A4
A3
A2
ADDMUXA
74LS244
8A
8Y
1A
1Y
1G
2G
DC15
DC8
DC7
DC0
DB68
687
686
685
684
74LS32
695
694
74LS04
696
DB29
/DPWROA
/ADDMUXA
/DPOE1A

FIG._29

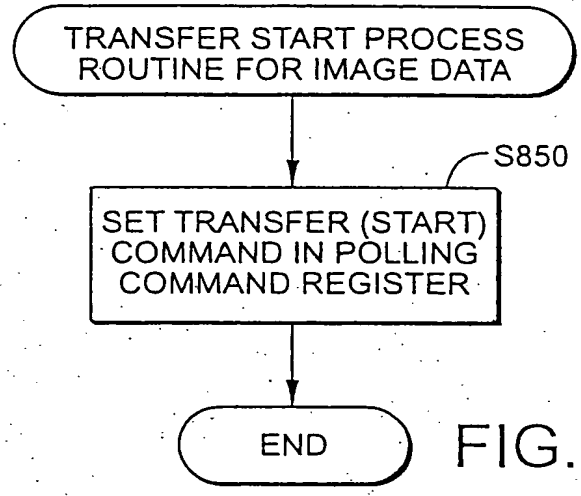

TRANSFER START PROCESS ROUTINE FOR IMAGE DATA
S850
SET TRANSFER (START) COMMAND IN POLLING COMMAND REGISTER
END

FIG._30

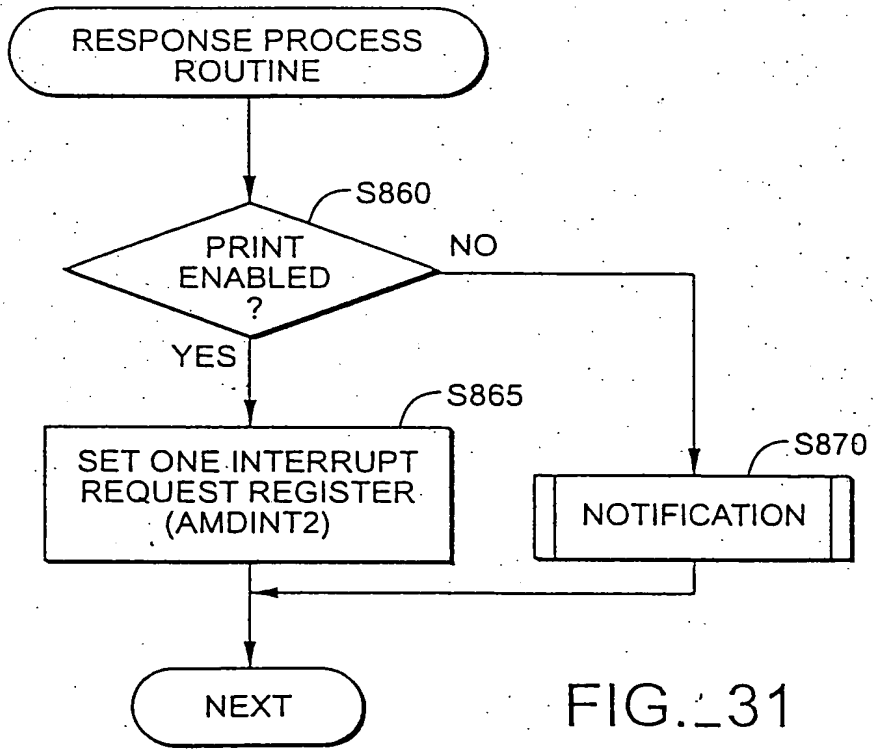

RESPONSE PROCESS ROUTINE
S860
PRINT ENABLED ?
NO
YES
S865
SET ONE INTERRUPT REQUEST REGISTER (AMDINT2)
S870
NOTIFICATION
NEXT

FIG._31

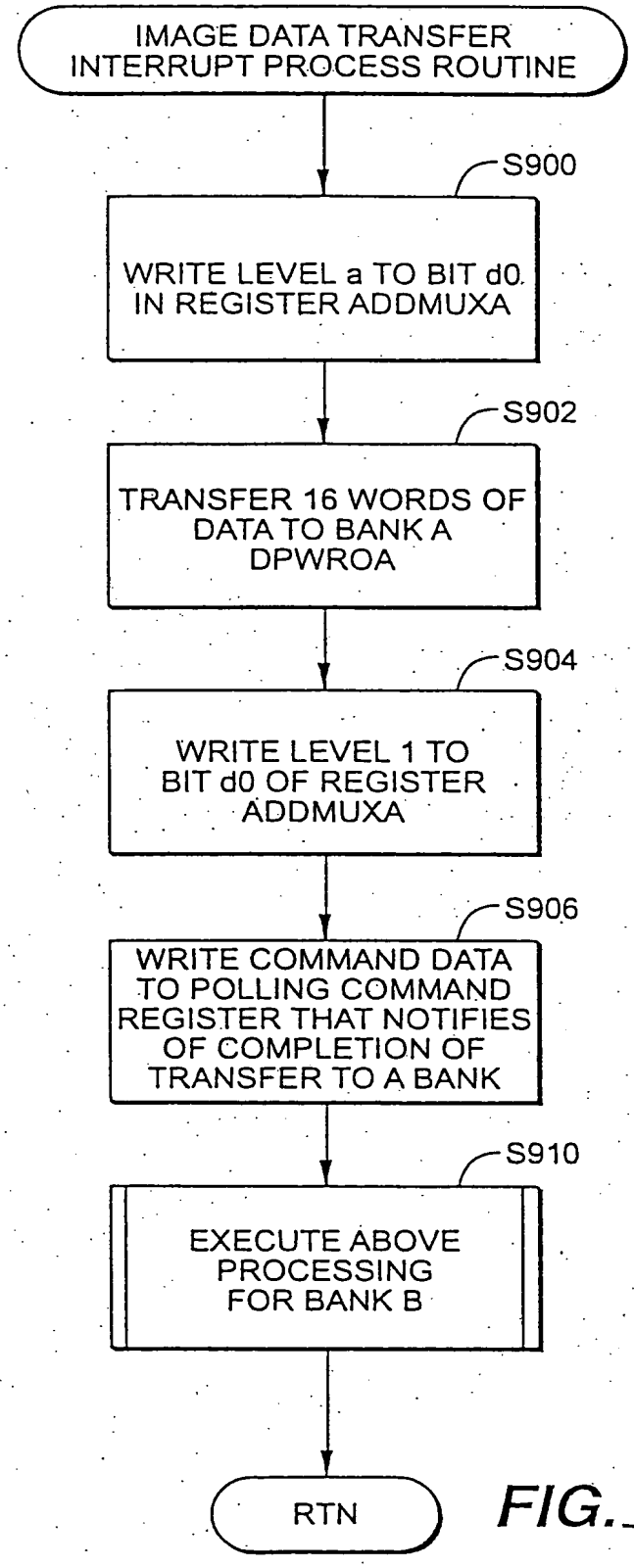


IMAGE DATA TRANSFER INTERRUPT PROCESS ROUTINE
S900
WRITE LEVEL a TO BIT d0 IN REGISTER ADDMUXA
S902
TRANSFER 16 WORDS OF DATA TO BANK A DPWROA
S904
WRITE LEVEL 1 TO BIT d0 OF REGISTER ADDMUXA
S906
WRITE COMMAND DATA TO POLLING COMMAND REGISTER THAT NOTIFIES OF COMPLETION OF TRANSFER TO A BANK
S910
EXECUTE ABOVE PROCESSING FOR BANK B
RTN

FIG._32

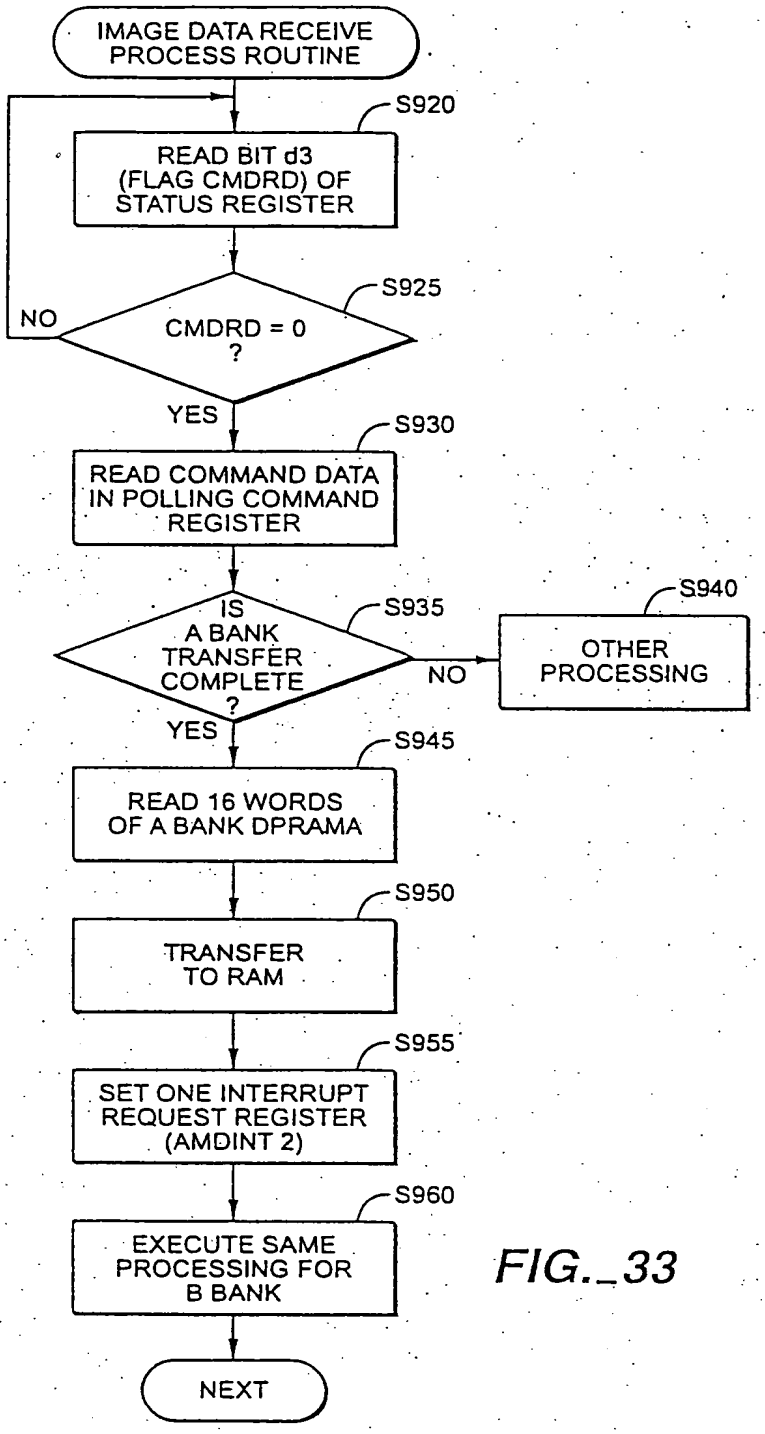


IMAGE DATA RECEIVE PROCESS ROUTINE
S920
READ BIT d3 (FLAG CMDRD) OF STATUS REGISTER
S925
NO
CMDRD = 0 ?
YES
S930
READ COMMAND DATA IN POLLING COMMAND REGISTER
S935
IS A BANK TRANSFER COMPLETE ?
NO
S940
OTHER PROCESSING
YES
S945
READ 16 WORDS OF A BANK DPRAMA
S950
TRANSFER TO RAM
S955
SET ONE INTERRUPT REQUEST REGISTER (AMDINT 2)
S960
EXECUTE SAME PROCESSING FOR B BANK
NEXT

FIG._33

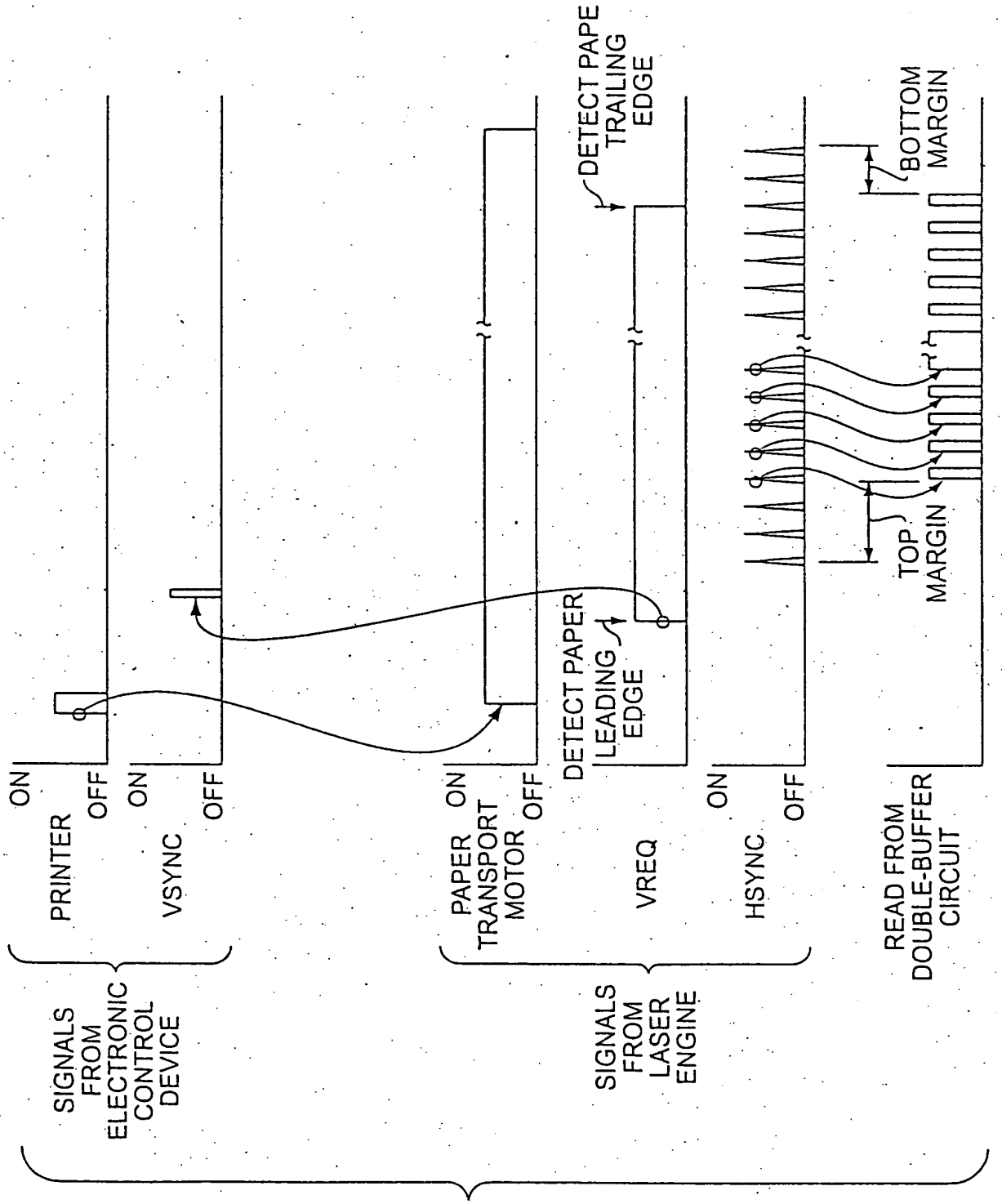

SIGNALS FROM ELECTRONIC CONTROL DEVICE
PRINTER
ON
OFF
VSYNC
ON
OFF
SIGNALS FROM LASER ENGINE
PAPER TRANSPORT MOTOR
ON
OFF
VREQ
DETECT PAPER LEADING EDGE
DETECT PAPE TRAILING EDGE
HSYNC
ON
OFF
TOP MARGIN
BOTTOM MARGIN
READ FROM DOUBLE-BUFFER CIRCUIT

FIG._34

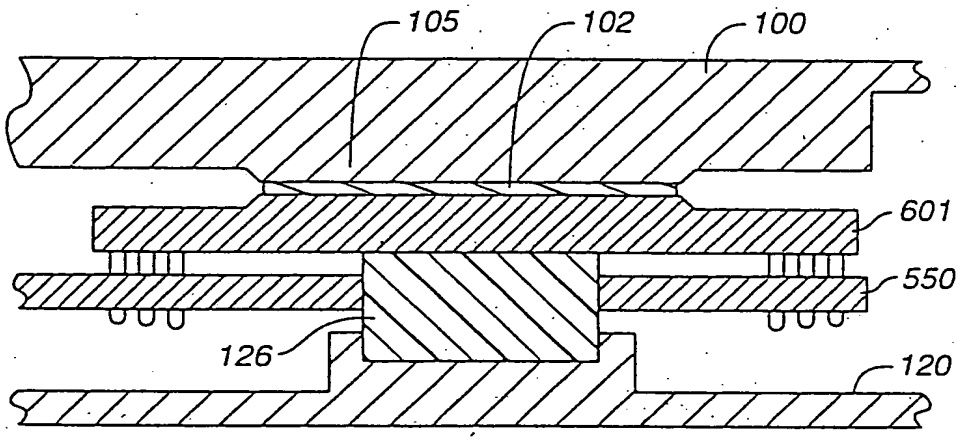


FIG._35